

1           23. (New) The method of claim 21, wherein the insulating liners are each  
2 disposed on an interconnect wall adjacent the gate to separate each of the local  
3 interconnects from the gate.

12 cont  
1           24. (New) The method of claim 21, wherein a source and drain are  
2 disposed by at least partially beneath the insulating liners.

1           25. (New) An integrated circuit including at least a pair of local  
2 interconnects with one interconnect on each side of a gate of a transistor, the  
3 integrated circuit being manufactured by a method comprising steps of:  
4           forming on a semiconductor substrate a thick insulating layer;  
5           forming at least a pair of spaced apart openings in the insulating layer  
6 adjacent the semiconductor substrate;  
7           forming a source in one of the openings and a drain in the other of the  
8 openings;  
9           filling each of the openings with a conductive material to form the local  
10 interconnects, the local interconnects being electrically coupled to the source  
11 and drain;  
12           removing a portion of the insulating layer to form a gate opening between  
13 the local interconnects;  
14           forming a gate dielectric on the semiconductor substrate in the gate  
15 opening; and  
16           forming the gate on the gate dielectric in the gate opening between the  
17 local interconnects.

1           26. (New) The integrated circuit of Claim 25, wherein the space between  
2 the pair of openings is one minimum photolithographic feature and the local  
3 interconnects are each one minimum photolithographic feature.

1           27. (New) The integrated circuit of Claim 25, wherein insulating spacers  
2 are each disposed on an interconnect wall adjacent the gate to separate each of  
3 the local interconnects from the gate.

Q2 1           ✓ 28. (New) The integrated circuit of Claim 25, wherein the source and  
2 drain are formed by implanting impurities in the pair of openings in the insulating  
3 layer.

1           ✓ 29. (New) The integrated circuit of Claim 25, wherein the portion of  
2 insulating layer removed to form the gate opening is removed by using a masking  
3 material with an opening in the masking material positioned between the pair of  
4 local interconnects.

1           ✓ 30. (New) The integrated circuit of Claim 29, wherein the opening in the  
2 masking material extends over but not beyond each of the pair of local  
3 interconnects.

1           ✓ 31. (New) The integrated circuit of Claim 30, wherein the opening in the  
2 masking material is positioned over an active region in the semiconductor  
3 substrate, the active region being surrounded by an isolation region, the opening  
4 in the masking material extending to or beyond the active region.

1           32. (New) The integrated circuit of Claim 25, wherein a conductive layer  
2 is formed on walls of the to line the spaced apart openings and a remainder of  
3 the spaced apart openings are filled with another conductive material.

1           33. (New) The integrated circuit of Claim 25, wherein the conductive  
2   layer is polysilicon and the another conductive material is tungsten.

1           34. (New) The integrated circuit of Claim 33, wherein the polysilicon is  
2   the origin for the impurities for the source and drain.

67  
End  
1           35. (New) The integrated circuit of Claim 25, wherein a barrier layer is  
2   formed on the walls of the spaced apart openings to line the opening and a  
3   remainder of the local interconnect opening is filled with a conductive material.

1           36. (New) The integrated circuit of Claim 35, wherein the barrier layer  
2   includes titanium nitride.

1           ✓ 37. (New) The integrated circuit of Claim 25, wherein an insulating etch  
2   stop layer is formed on semiconductor substrate before forming the thick  
3   insulating layer.

1           ✓ 38. (New) The integrated circuit of Claim 37, wherein the etch selectivity  
2   of the etch stop layer is different from the etch selectivity of the insulating layer.

---

#### REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.